Remarks

Thorough examination by the Examiner is noted and appreciated.

Support for the amended claims is found in the previously presented claims, the Specification and the Figures.

No new matter has been added.

For example support for the amendments and new claims is found in the original and previously presented claims as well as the Figures including Figure 1E:

Claim Rejections under 35 USC 103

1. Claims 18-22, 24, 25, 27-30, 32-35, and 38-45, 47, 49 and 50 stand rejected under 35 USC Section 103(a) as being unpatentable over Tamaru (US 2003/0030146) in view of Chen et al. (6,784,096).

Tamaru disclose a **single contact layer** (16) with contact interconnect structures (18; e.g., Figures 6, 7) penetrating the

single contact layer (16). Tamaru clearly disclose forming contact holes **(openings)** (17) in the single contact layer (16) and forming metal W plugs (18) (TiN barrier layer and W metal plug in the contact holes (paragraph 0079). Tamaru then disclose forming **wiring grooves (lines)** for forming **first layer Cu wiring** (24) (also known in the art to one of ordinary skill as a **metallization layer** (as **opposed to a contact openings in a contact layer**) including a "**high melting metal nitride" barrier layer** (TiN, Ti/TiN, WN, TaN, and Ta/TaN paragraph 0088) separating the **contact metal plugs** and the **Cu wiring in the metallization layer above the contact layer** (16) (see paragraphs 0080, 0087, 0088; Figures 6 and 7). Thus, in cross section the Cu **wiring** (24) makes physical contact with the "**high melting metal nitride" barrier layer on the contact interconnect structure** i.e., barrier layer on contact **plugs** (**metal filled holes**) (18) and (see also Abstract and claim 1).

Therefore Tamaru fails to disclose Applicants invention including those elements in **bold type**:
With respect to claim 18:

"A **contact interconnect structure** comprising:

a semiconductor substrate comprising CMOS devices including active contact regions;

a first contact layer overlying the active contact regions comprising a first plurality of metal filled contact openings extending through the first contact layer thickness to the active contact regions;

a second contact layer overlying the first contact layer comprising a second plurality of metal filled contact openings, each of said second plurality of metal filled contact openings extending through the second contact layer thickness to physically contact a major metal filling portion of a respective one or more of the first plurality of metal contact filled openings;

wherein, the first plurality and the second plurality of metal filled contact openings **form a physically continuous contact interconnect structure**, said first and second metal filled contact openings having an aspect ratio of less than about 4.5 with respect to a respective contact layer, **said contact**

interconnect structure connecting said active contact regions to overlying wiring circuitry comprising metallization layers, said first and second metal filled contact openings not comprising wiring grooves."

With respect to claim 32:

36. A contact interconnect structure comprising:

at least first and second stacked contact layers comprising a respective first and second plurality of metal filled contact openings, extending through ~~the~~ respective first and second contact layers, each of said second plurality of metal filled contact openings extending to a respective contact region comprising an active transistor region, **each of said first plurality of metal filled contact openings physically contacting a respective one of said second plurality of metal filled contact openings, said physical contact through major metal filling portions comprising said first and second plurality of metal filled contact openings;**

wherein, the first plurality and the second plurality of

metal filled contact openings comprise a bottom portion having a maximum width of less than about 70 nanometers, said first and second metal filled contact openings having an aspect ratio of less than about 3.3 with respect to a respective contact layer, **said first and second plurality of said metal filled contact openings connecting said active contact regions to overlying wiring circuitry** comprising metallization layers, **said first and second plurality of said metal filled contact openings not comprising wiring grooves**.

Examiner is apparently erroneously (and contrary to the understanding of the structures and plain meaning of Applicants claim language to one of ordinary skill (as is evidenced by the teachings of Tamaru) equating the metallization layer (including wiring grooves) of Tamaru as equivalent to Applicants second contact layer (including the second metal filled contact openings).

Applicants have therefore further amended their claims to explicitly specify that the first and second metal filled contact openings do not comprise wiring grooves in an effort to overcome Examiners apparent interpretation of Applicants claim language.

Moreover, as noted above, Tamaru nowhere discloses or suggests that the Cu filled wiring grooves **physically contact** a major metal filling portion of the metal filled (W) contact plugs (i.e., tungsten). Rather Tamaru clearly disclose **a metal nitride barrier layer between the two major metal filling portions of the structures** (see paragraphs 0080, 0087, 0088; Figures 6 and 7).

In contrast to Tamaru, and in **non-analogous art**, Chen et al. disclose a method of **forming a barrier layer to line vias** where the **vias** are disclosed to have a width less than 70 nm or an aspect ratio greater than about 3:1 (see Abstract; Figures).

"Embodiments of the present invention provide **methods and apparatus for forming barrier layers in high aspect ratio vias (e.g., vias having aspect ratios of 3:1, 4:1, 5:1 or higher)** and/or **vias having via widths of about 0.065-0.2 microns or below**. It will be understood that the invention also may be employed to form barrier layers in lower aspect ratio and/or wider vias. Each embodiment allows a relatively thick barrier layer to be deposited on the sidewalls of a via with little or no barrier layer coverage on the bottom of the via. Adequate diffusion resistance and/or mechanical strength thereby may be provided without significantly increasing the contact resistance of the interconnect formed with the via."

Even assuming *arguendo*, a proper motivation to modify Tamaru based on the teachings of Chen et al., such modification **fails to produce Applicants invention**.

As noted above, Tamaru nowhere discloses metal filled contact openings **physically contacting one another** but rather discloses **Cu filled wiring grooves** in a metallization layer contacting a **metal nitride barrier layer** formed **between** contact openings (plugs) and the **Cu filled wiring grooves.**

"**First**, there must be some **suggestion or motivation**, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. **Second**, there must be a **reasonable expectation of success**. **Finally**, the prior art reference (or references when combined) **must teach or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device." *Ex parte Chicago Rawhide Mfg. Co., 223 USPQ 351, 353*

(Bd. Pat. App. & Inter. 1984).

With respect to claims 47, and 49 Examiner is mistaken that Tamaru discloses "The contact interconnect structure of claim 38, wherein the first plurality and the second plurality of metal filled contact openings comprise the same material."

Rather, as noted above, Tamaru discloses **Cu filled wring groves** and nowhere discloses Cu contact plugs, and further discloses a metal nitride barrier layer between the Cu wiring and the W contact plugs.

2. Claims 26 and 36 stand rejected under 35 USC Section 103(a) as being unpatentable over Tamura, above in view of Chen et al., above, and further in view of Ono (IEE Trans on Electronic Devices, pg 1822 Vol. 42, No. 10, 1995).

Applicants reiterate the comments made above with respect to Tamura and Chen et al.

Even assuming *arguendo*, a proper motivation to further

modify Tamura with the teachings of Ono, the further fact that Ono discloses a gate length of less than about 45 nm without a corresponding disclosure or teaching of a contact interconnect structure does not further help Examiner in producing Applicants invention.

"**First**, there must be some **suggestion or motivation**, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. **Second**, there must be a **reasonable expectation of success**. **Finally**, the prior art reference (or references when combined) **must teach or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)*.

"The fact that references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a prima facie case of obviousness without some objective reason to combine the teachings of the references." *Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App.*

& Inter. 1993).

Conclusion

The cited references, singly or in combination fail to produce or suggest the elements of Applicants invention, and therefore fail to make out a *prima facie* case of obviousness.

Applicants have further amended their claims to further define over the prior art. Applicants respectfully request favorable consideration of their claims.

Based on the foregoing, Applicants respectfully submit that Applicants Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants= representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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